Claims

[c1] What is claimed is:

1. A method for controlling a system bus for a computer system, the computer system comprising a bus master electrically connected to the bus, the method comprising:

(a) receiving an entry command transmitted by the bus master via the bus;

(b)sequentially queuing every entry command transmitted from the bus master to a memory;

(c) replying with a corresponding acknowledge signal to the bus master through the bus, according to sequential store of each queued entry command in the memory;

(d) the bus master outputting a control signal to release access of the bus and returning to be in a stand-by mode as soon as receiving each said acknowledge signal;

(e)generating a corresponding executing result by way of sequential implementation of each queued entry command stored in the memory; and

(f) enabling the bus master to catch each executing result generated in said step (e).

[c2] 2.The method of claim 1 wherein the computer system

further comprises a system bus controller.

[c3] 3.The method of claim 2 wherein the system bus controller comprises:
a bus slave interface connected to the bus for receiving the entry command transmitted from the bus master;
a master queue used with the memory for storing each queued entry command in step(b)
a queue entries executor for sequentially implementing each queued entry command stored in said master queue in step(e) to generate a corresponding executing result; and
a queue management unit for managing queue and update of each entry command in the master queue and transmission of the acknowledge signal in the step(c).

[c4] 4.The method of claim 3 wherein the system bus controller further comprises a bus master interface electrically connected to the bus, for actively outputting the executing result of step(e) to the bus master.

[c5] 5.The method of claim 3 wherein each executing result in response to each queued entry command is capable of being further queued in a specific address defined within the master queue.

[c6] 6.The method of claim 5 wherein the system bus con-

troller further comprises:
a polling module for periodically detecting whether there is any executing result found in the master queue, with response to each queued command, so as to enable the bus master to catch the existing executing result.

[c7] 7.The method of claim 5 wherein the system bus controller further comprises:
an interrupt controller electrically connected to the queue management unit, which is triggered to enable the bus master to catch an executing result , by means that the queue management unit stores the executing result into the master queue.

[c8] 8.The method of claim 1 wherein step (f) further comprises: periodically detecting whether there is any executing result corresponding to the entry command is generated thereby enabling the bus master to catch the executing result.

[c9] 9.The method of claim 1 wherein step (f) further comprises:
after generating each executing result corresponding to the entry command, correspondingly generating and transmitting an interrupt control signal to the bus master thereby enabling the bus master to catch the executing result.

[c10] 10.A system bus controller suitable for a computer system having a bus and a bus master electrically connected to the bus, the system bus controller comprising:
a bus slave interface electrically connected to the bus and receiving each entry command transmitted from the bus master through the bus;
a master queue capable of storing the entry commands received by the bus slave interface;
a queue entries executor capable of executing the entry commands stored in the master queue thereby generating a corresponding executing result;
a bus master interface electrically connected to the bus and outputting the executing result generated by the queue entries executor; and
a queue management unit, respectively connected to the bus master interface, the bus slave interface, the queue entries executor and the master queue, being capable of managing the queue of all entry commands in the master queue and outputting a acknowledge signal to the bus master with regard to each received entry command.

[c11] 11.The system bus controller of claim 10 wherein the master queue is allocated in a dynamic random access memory.

[c12] 12. A system bus controller of a computer system having

a bus and a bus master electrically connected to the bus, the system bus controller comprising:
a bus slave interface electrically connected to the bus, being capable of receiving each entry command transmitted from the bus master through the bus;
a master queue for storing therein entry commands received by the bus slave interface;
a queue entries executor for executing the entry commands stored in the master queue to generate a corresponding executing result;
a queue management unit, respectively connected to the bus master interface, the bus slave interface, the queue entries executor and the master queue, being capable of managing the queue of each entry command in the master queue and outputting an acknowledge signal to the bus master, with regard to the each received command, thereby facilitating return of the bus master to be in a stand-by mode; and
a device capable of outputting a signal to enable the bus master to catch the corresponding executing result when the executing result generated from the queue entries executor is detected by the device, through the queue management unite.

[c13] 13.The system bus controller of claim 12 wherein the master queue is allocated in a dynamic random access

memory.

[c14] 14.The system bus controller of claim 12 wherein the device is a polling module that detects whether any executing result exists with regard to the entry command through the queue management unit.

[c15] 15.The system bus controller of claim 12 wherein the device is an interrupt controller that can be triggered by the queue management unit after an executing result is generated, so as to enable the bus master to catch the executing result.